Intel x86 CPU architecture

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Vilnius, 2020

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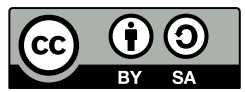
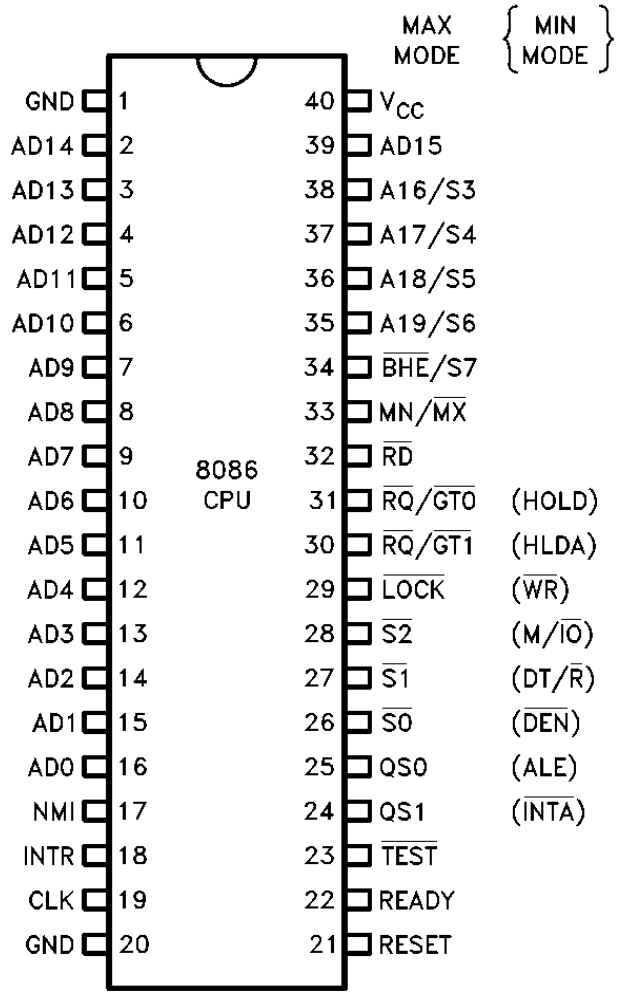


What is a processor architecture?

Architecture visible to programmer:

- The CPU registers visible to programmer
- Memory addressing
- Data formats
- Processor instruction set
- Input-output
- Interrupt processing

A bit of history



(Intel 1990)

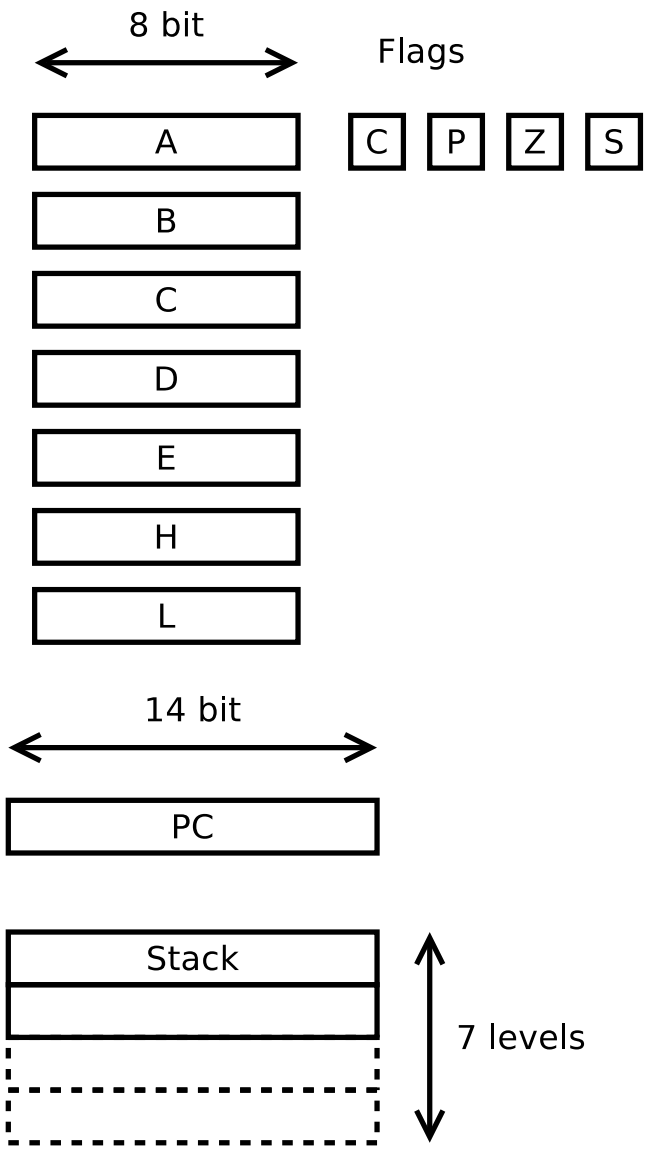
- 1974 8080 8-bit; Addr: 16 bit (64K)
- 1978 8086, 8088 16-bit; Addr: 20 bit (1MB)
- 1982 Intel® 286 16-bit (protected memory); Addr: 24 bit (16MB)
- 1985 Intel386™ 32-bit; Addr: 32 bit (4GB);
- 1989 Intel486™ 32-bit (+FPU, more instr.); Addr: 32 bit (4GB);
- 1993 Intel® Pentium® 32-bit (faster, more instr.); Addr: 32 bit (4GB);
- 1995-1999 The P6 Family of Processors 32-bit; Addr: 32 bit (4GB);
- **1999 AMD Opteron 64-bit; Addr: up to 64 bit**
- 2001-2007 The Intel® Xeon® 64-bit, Addr: up to 64 bit.

(Intel 2020)

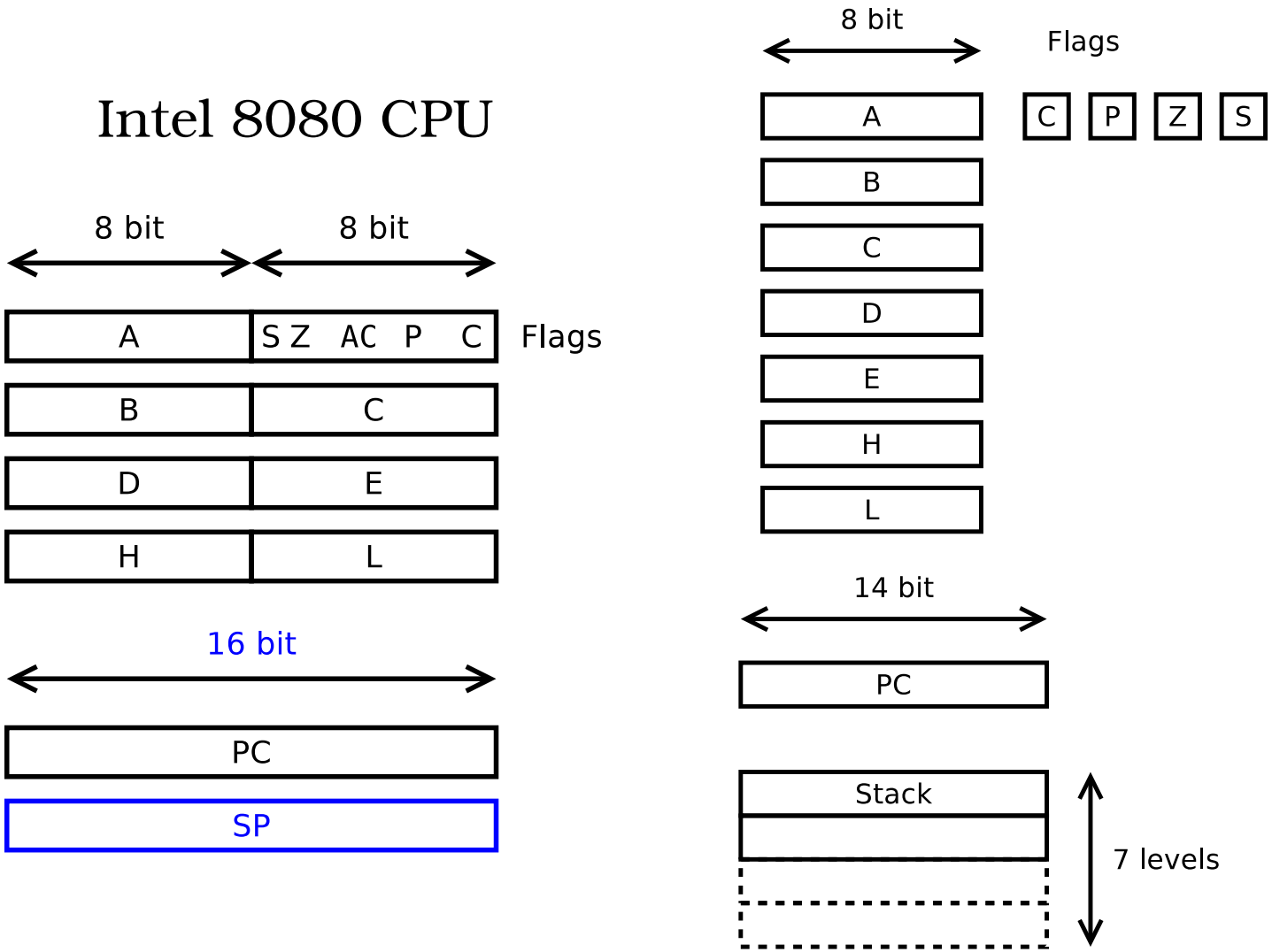
Notational Conventions

- `#GP(0)` An instruction exception—in this example, a general-protection exception with error code of 0.
- `1011b` A binary value—in this example, a 4-bit value.
- `DEAD_BEEFh` A hexadecimal value. Underscore characters may be inserted to improve readability.
- `128` Decimal number, unless the context indicates otherwise.
- `7:4` A bit range, from bit 7 to 4, inclusive. The high-order bit is shown first. Commas may be inserted to indicate gaps.

Registers (x86) – history: 8008

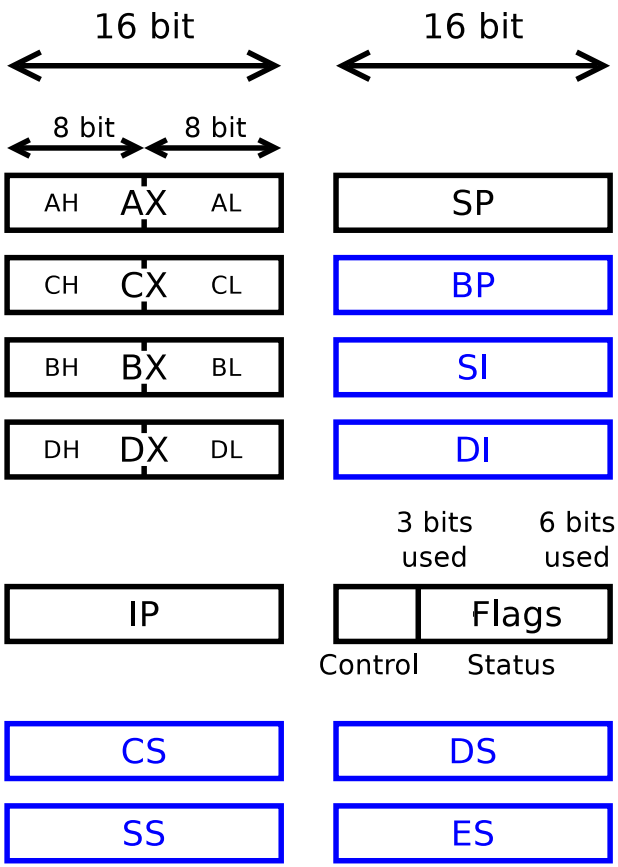


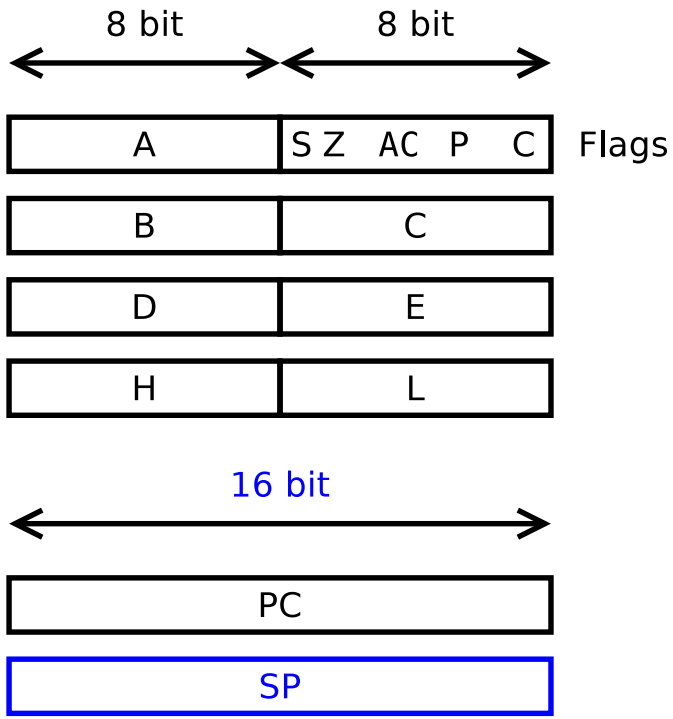
Registers (x86) – history: 8080



Registers (x86)

Intel 8086 CPU



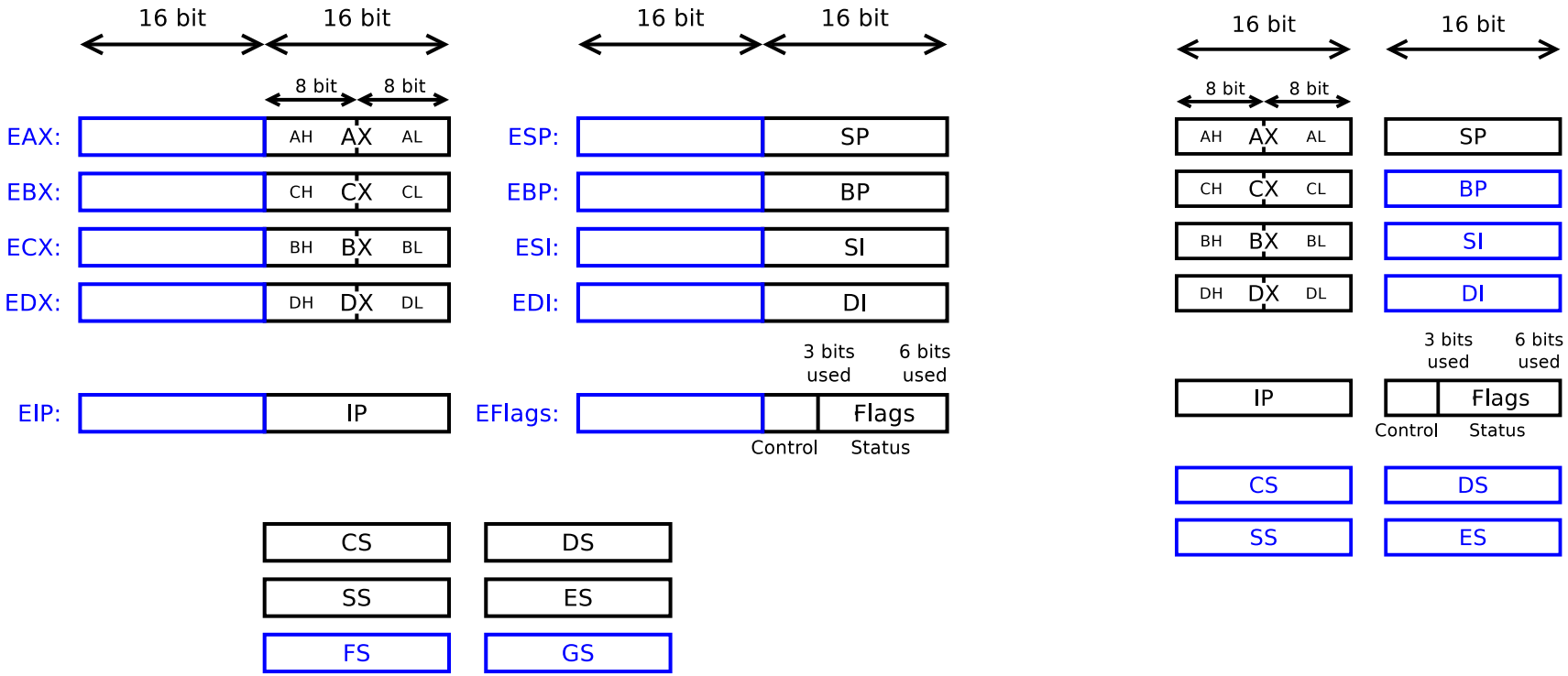


(Intel 1979)

https://www.youtube.com/watch?v=7xwjjolDnwg

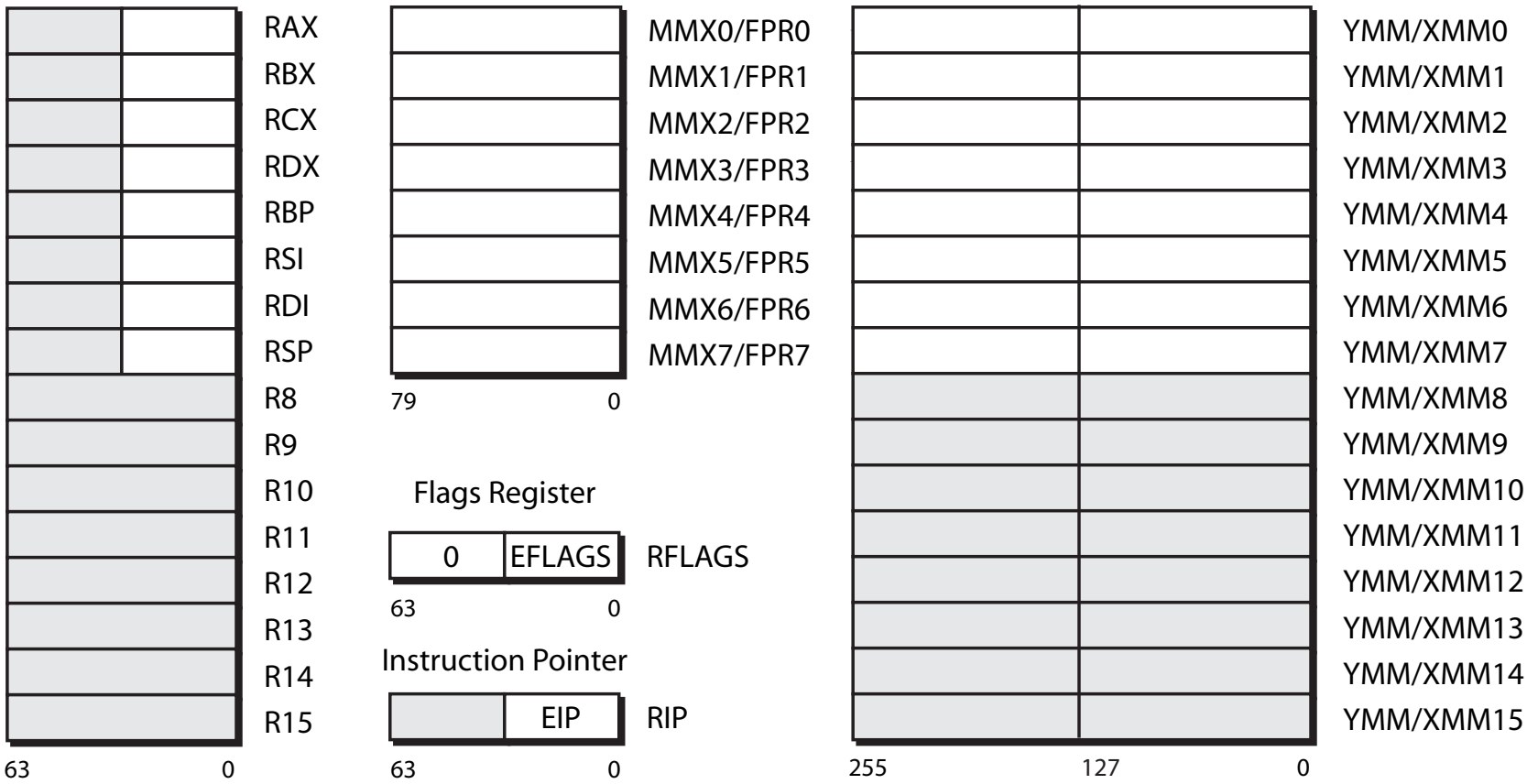
Registers (80386)

Intel 80386 CPU



https://www.youtube.com/watch?v=7xwjjolDnwg

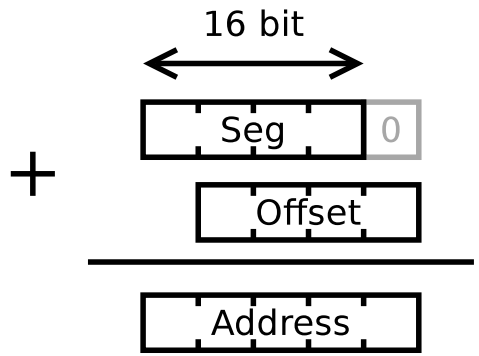
Registers (x86_64)



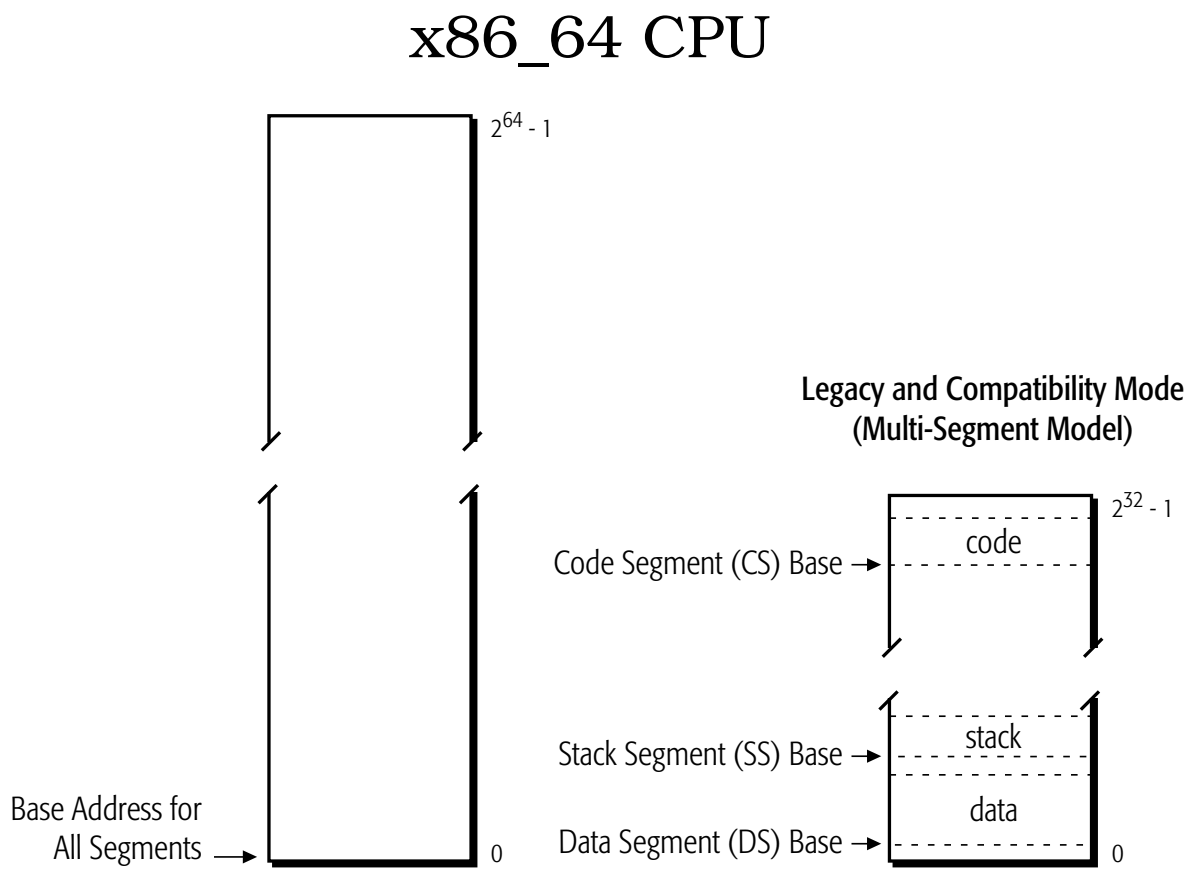
(AMD 2017), here and further: reproduced with AMD permission

Segmented addressing

Segment address is shifted by 4 bits and added to the offset:

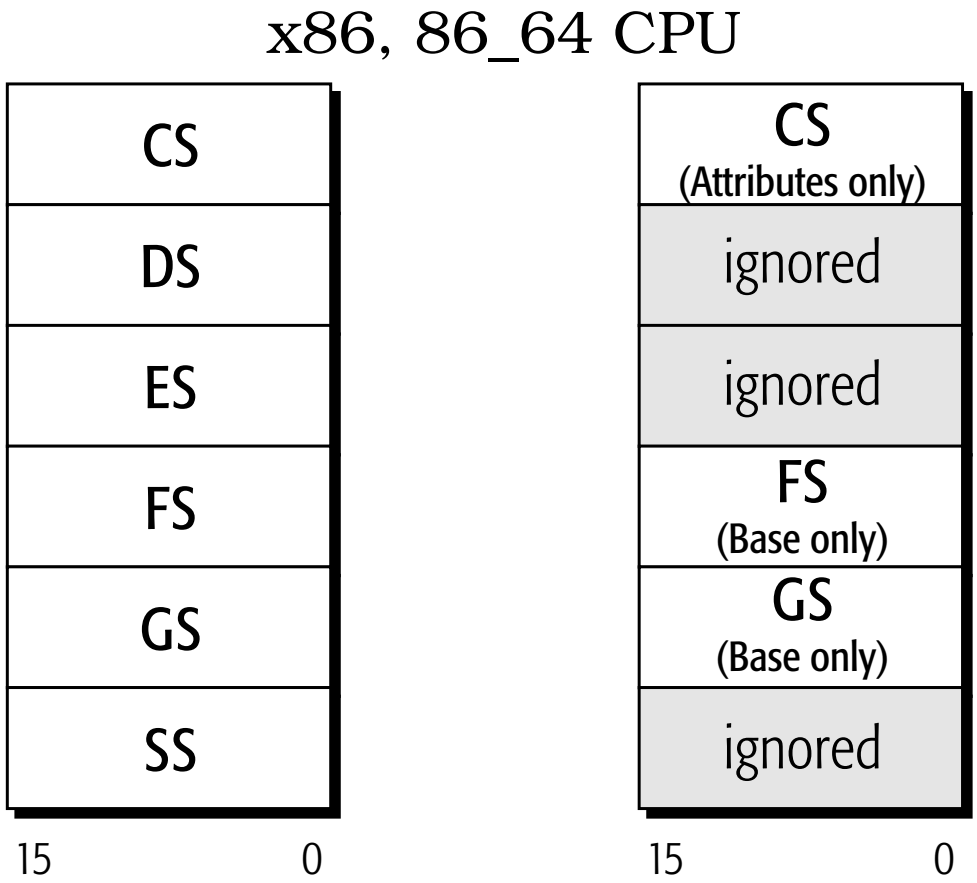


Memory layout



(AMD 2017)

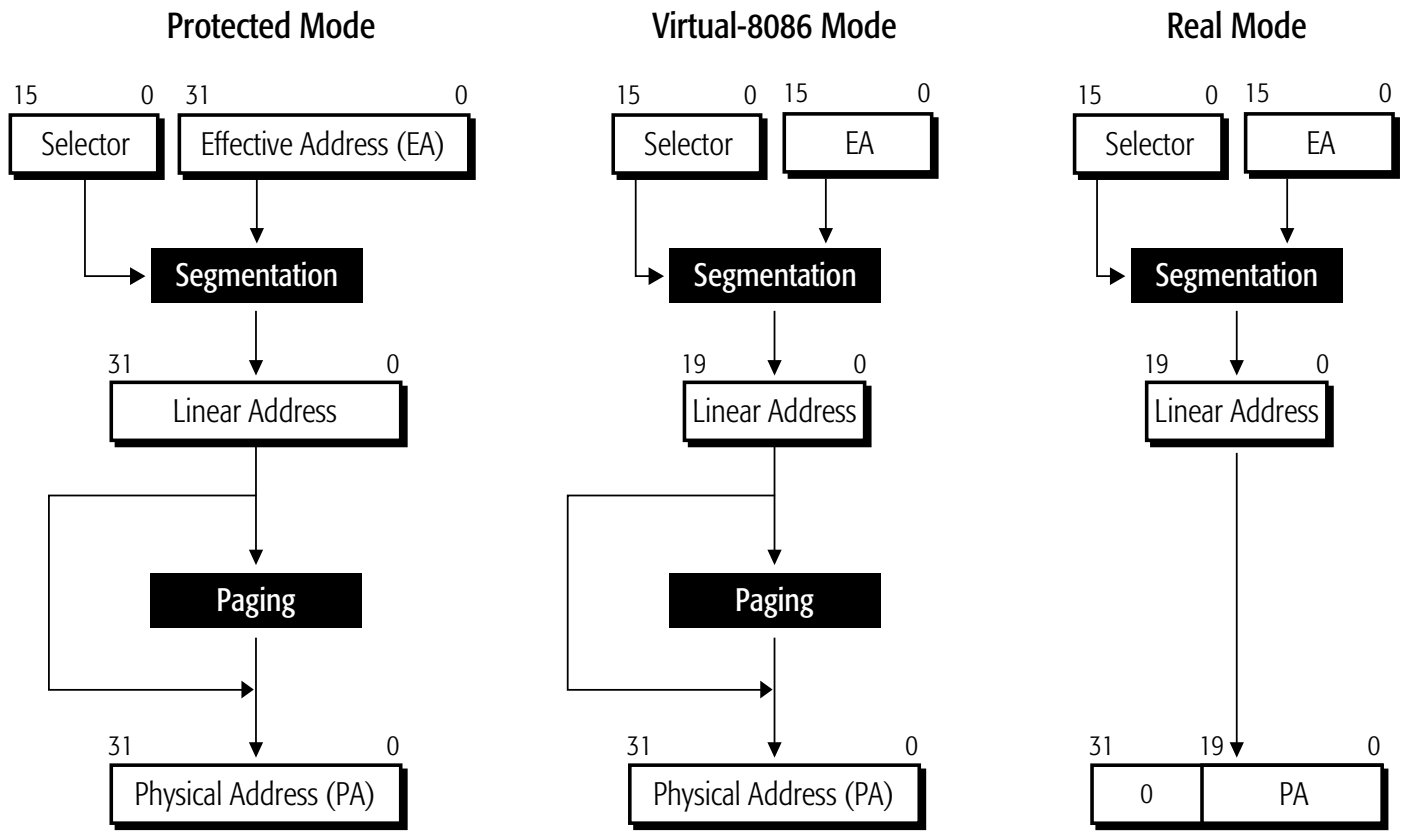
Segment Registers



(AMD 2017)

Legacy mode memory management

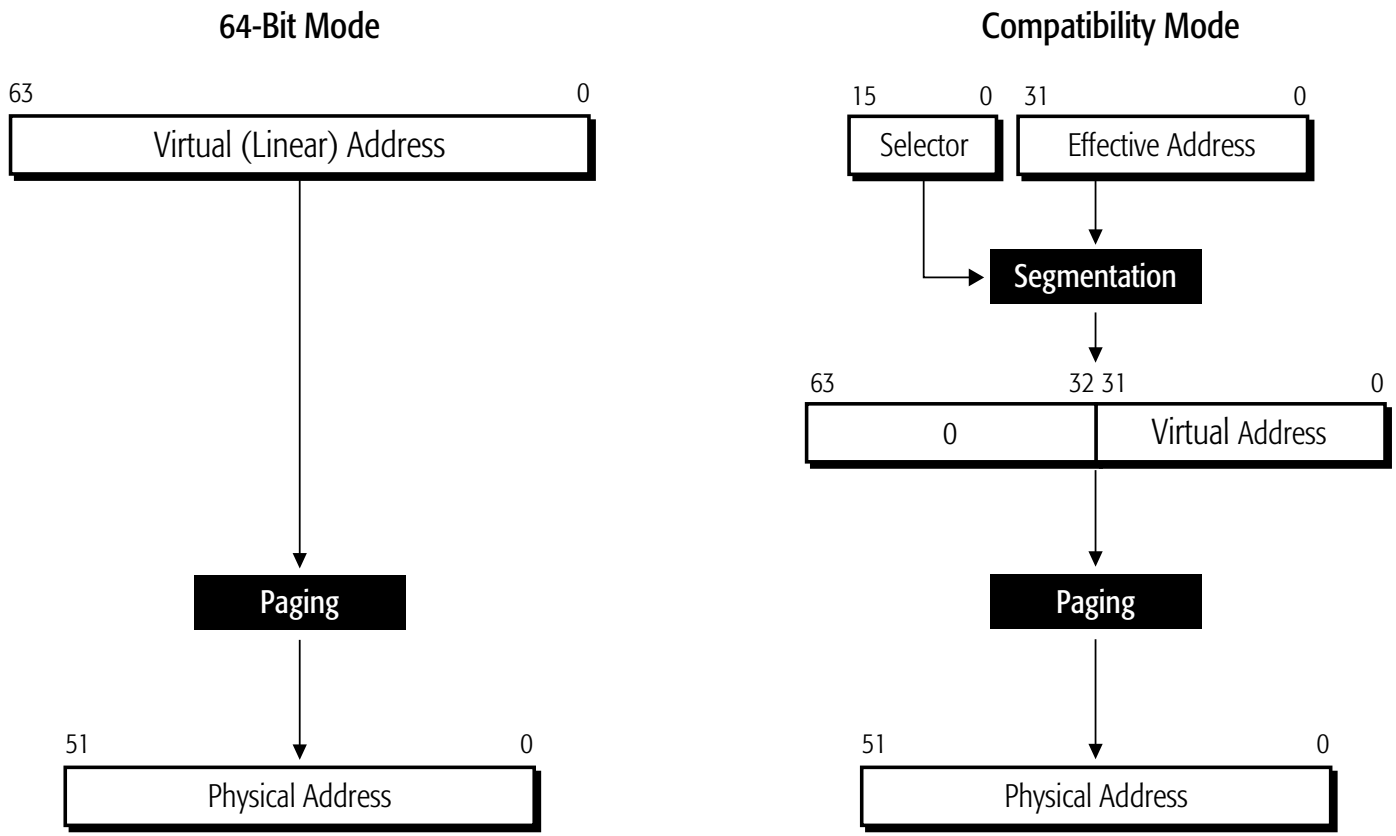
x86, 86_64 CPU



(AMD 2017)

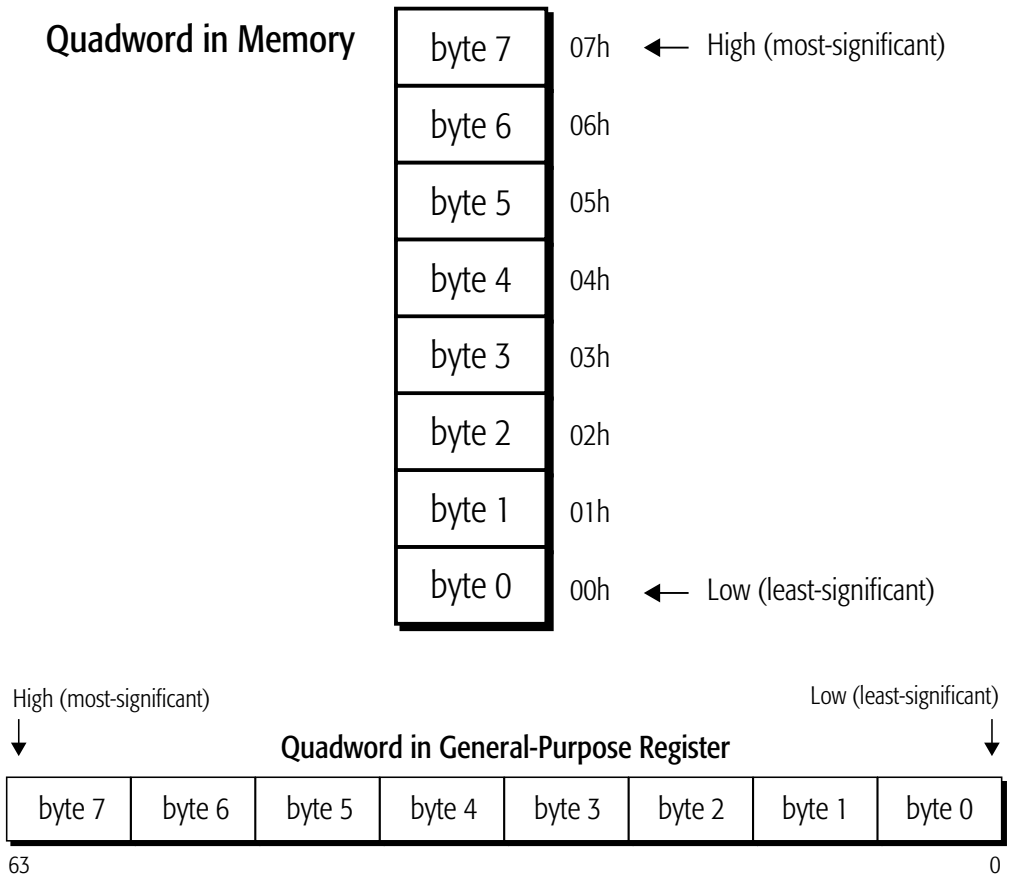
Long-mode memory management

x86, 86_64 CPU



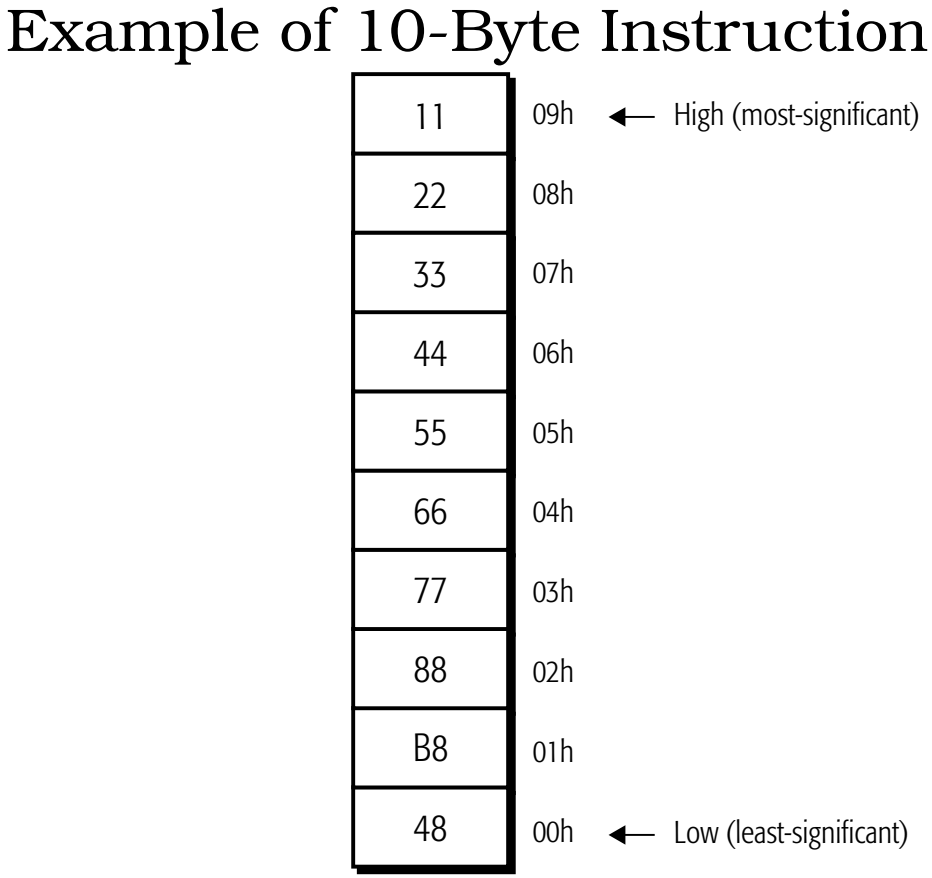
(AMD 2017)

Byte order



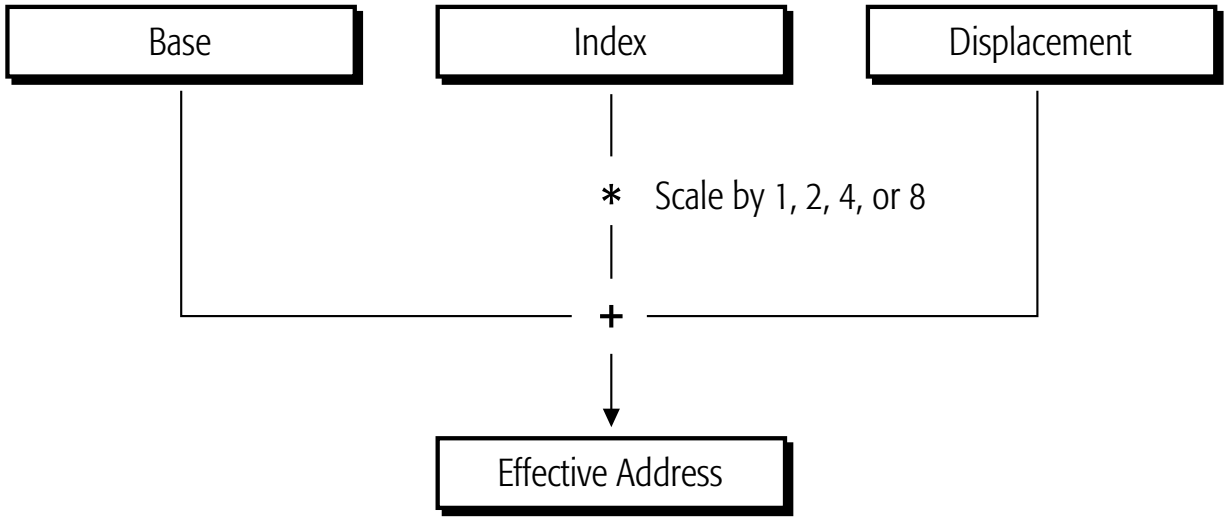
(AMD 2017)

Instructions in memory



(AMD 2017)

Complex address calculation (protected mode)

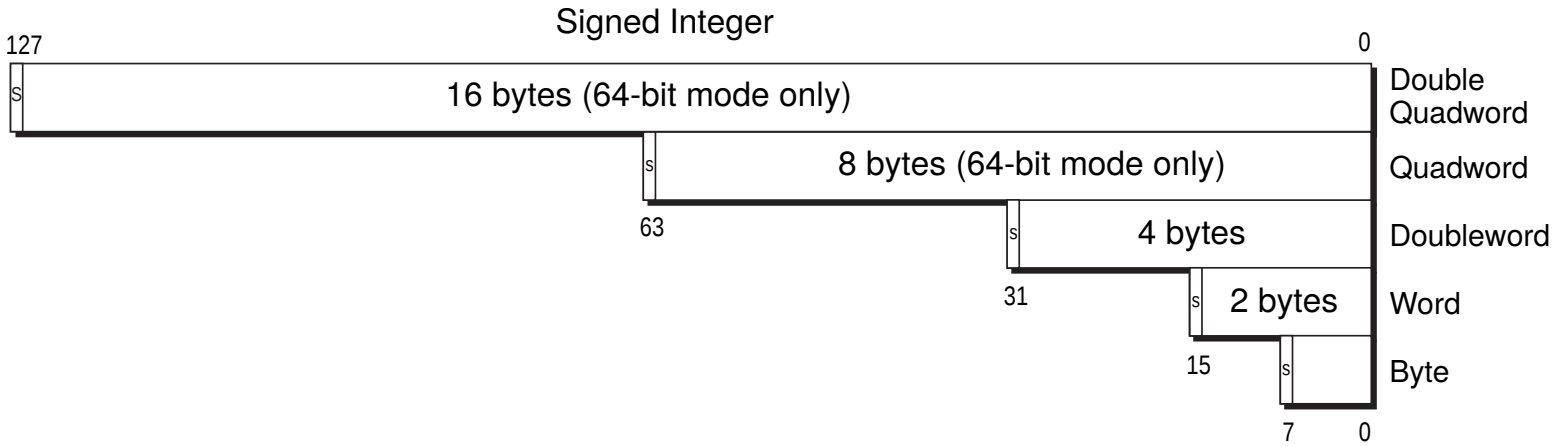


(AMD 2017)

Near and far pointers

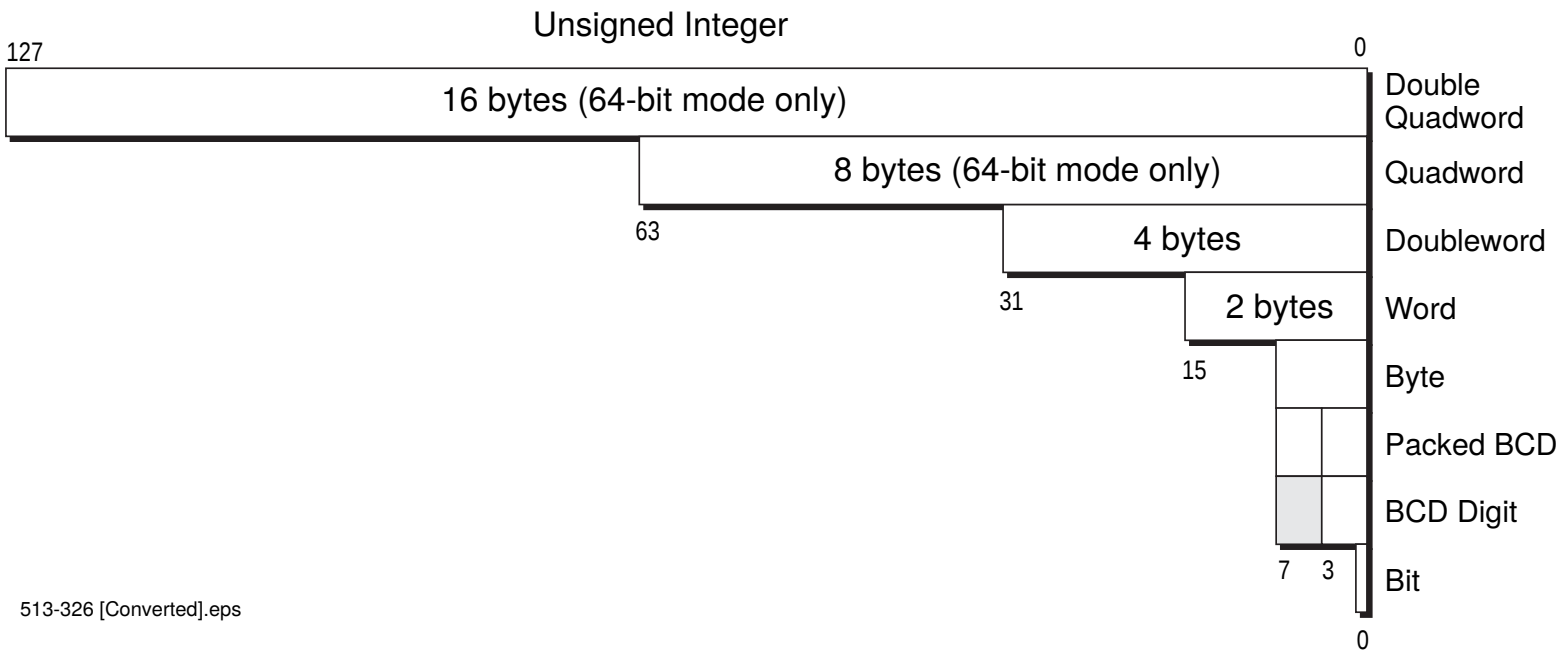
(AMD 2017)

Basic data types



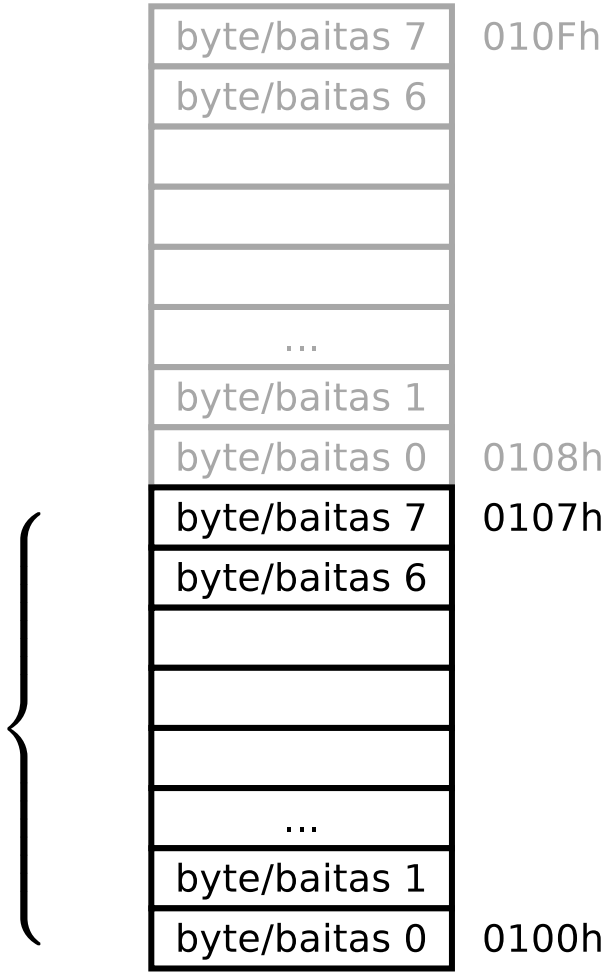
(AMD 2017)

Basic data types

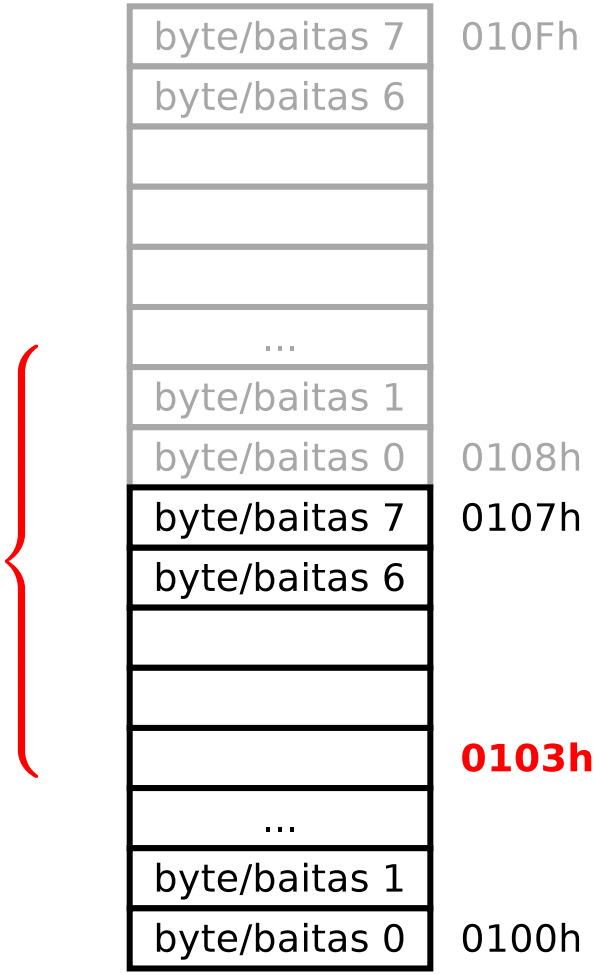


(AMD 2017)

Memory alignment



Memory alignment



Take-home message

- The x86 processor architecture stayed compatible (on the binary code level!) with the original 8086/8088 for more than 40 years (!)
- Aligned memory access is as a rule faster for all CPU architectures and required for some of them
- The x86_64 architecture features flat memory model, 16 64-bit general purpose registers, 16 vector registers and 8 floating point registers

References

AMD (Dec. 2017). *AMD64 Architecture Programmer's Manual, Volume 1: Application Programming, revision 3.22*. AMD. URL: https://www.amd.com/system/files/TechDocs/24592.pdf.

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